Arria 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® 10 devices.

Arria 10 devices are offered in extended and industrial grades. Extended devices are offered in –E1 (fastest), –E2, and –E3 speed grades. Industrial grade devices are offered in the –I1, –I2, and –I3 speed grades.

The suffix after the speed grade denotes the power options offered in Arria 10 devices.

- L—Low static power
- S—Standard power
- M—Enabled with the V_{CC} PowerManager feature (you can power V_{CC} and V_{CCP} at nominal voltage of 0.90 V or lower voltage of 0.83 V)

For more information about the densities and packages of devices in the Arria 10 family, refer to the *Arria 10 Device Overview*.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria 10 devices.

Operating Conditions

Arria 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria 10 devices, you must consider the operating requirements described in this section.

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Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

Conditions outside the range listed in Table 1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	—	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power	—	–0.50	1.34	V
V_{CCH_GXB}	Transmitter output buffer power	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.27	V
V_{CCIO_HPS}	HPS I/O buffers power supply	3V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
$V_{CCIOREF\_HPS}$	HPS I/O pre-driver power supply	—	–0.50	2.46	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
I_{OUT}	DC output current per pin	—	–25	25	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.24 V for LVDS I/O can only be at 2.24 V for ~26% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 2.6 years.

Table 2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Table 2. Maximum Allowed Overshoot During Transitions for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O	3V I/O		
Vi (AC)	AC input voltage	2.19	3.60	100	%
		2.24	3.65	26	%
		2.29	3.70	8	%
		2.34	3.75	3	%
		2.39	3.80	1	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria 10 devices.

Table 3 lists the steady-state voltage values expected from Arria 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 3. Recommended Operating Conditions for Arria 10 Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage power supply	Standard and low power	0.87	0.9	0.93	V
		V_{CC} PowerManager (1)	0.8, 0.87	0.83, 0.9	0.86, 0.93	V
		SmartVID	0.8	—	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	Standard and low power	0.87	0.9	0.93	V
		V_{CC} PowerManager (1)	0.8, 0.87	0.83, 0.9	0.86, 0.93	V
		SmartVID	0.8	—	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.95 V	0.92	0.95	0.98	V

Table 3. Recommended Operating Conditions for Arria 10 Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	(3)	1.35	(3)	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	(3)	1.2	(3)	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V
V_I	DC input voltage	3V I/O	–0.3	—	3.6	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
		Military	–55	—	125	°C
t_{RAMP} (4)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 3:

(1) You can operate V_{CC} PowerManager devices at either 0.83 V or 0.9 V. Power V_{CC} and V_{CCP} at 0.9 V to achieve –1 speed grade performance. Power V_{CC} and V_{CCP} at 0.83 V to achieve lower performance using the lowest power.

(2) If you do not use the design security feature in Arria 10 devices, connect V_{CCBAT} to a 1.5-V or 1.8-V power supply. Arria 10 power-on reset (POR) circuitry monitors V_{CCBAT}. Arria 10 devices do not exit POR if V_{CCBAT} is not powered up.

(3) For minimum and maximum voltage values, refer to the "I/O Standard Specifications" section.

(4) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Table 4 and Table 5 list the recommended operating conditions for Arria 10 transceiver power supplies.

Table 4. Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Condition (2)	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip ≤17.4 Gbps Or Backplane (1) ≤16.0 Gbps	0.970	1.0	1.030	V
		Chip-to-Chip ≤11.3 Gbps Or Backplane (1) ≤10.3125 Gbps	0.870	0.9	0.930	V

Table 4. Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices—*Preliminary (Part 2 of 2)*

Symbol	Description	Condition (2)	Minimum	Typical	Maximum	Unit
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip ≤17.4 Gbps Or Backplane (1) ≤16.0 Gbps	0.970	1.0	1.030	V
		Chip-to-Chip ≤11.3 Gbps Or Backplane (1) ≤10.3125 Gbps	0.870	0.9	0.930	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.710	1.8	1.890	V

Note to Table 4:

(1) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(2) These data rate ranges vary depending on the transceiver speed grade. Refer to Table 19 for exact data rate ranges.

Table 5. Transceiver Power Supply Operating Conditions for Arria 10 GT Devices—*Preliminary*

Symbol	Description	Condition (3)	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip < 28.3 Gbps (1) Or Backplane (2) < 17.4 Gbps	1.070	1.1	1.130	V
		Chip-to-Chip < 15 Gbps Or Backplane (2) < 14.2 Gbps	0.970	1.0	1.030	V
		Chip-to-Chip < 11.3 Gbps Or Backplane (2) < 10.3125 Gbps	0.870	0.9	0.930	V
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip < 28.3 Gbps (1) Or Backplane (2) < 17.4 Gbps	1.070	1.1	1.130	V
		Chip-to-Chip < 15 Gbps Or Backplane (2) < 14.2 Gbps	0.970	1.0	1.030	V
		Chip-to-Chip < 11.3 Gbps Or Backplane (2) < 10.3125 Gbps	0.870	0.9	0.930	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power supply	—	1.710	1.8	1.890	V

Notes to Table 5:

(1) 28.3 Gbps is the maximum data rate for GT channels. 17.4 Gbps is the maximum data rate for GX channels.

(2) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(3) These data rate ranges vary depending on the transceiver speed grade. Refer to Table 21 for exact data rate ranges.

Table 6 lists the steady-state voltage and current values expected from Arria 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. HPS Power Supply Operating Conditions for Arria 10 SX Devices (1)—*Preliminary*

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	HPS processor speed = 1.2 GHz	0.87	0.9	0.93	V
		HPS processor speed = 1.5 GHz	0.92	0.95	0.98	V
V_{CCIO_HPS}	HPS I/O buffers power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
$V_{CCIOREF\_HPS}$	HPS I/O pre-driver power supply	—	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V

Note to Table 6:

(1) Refer to Table 3 for the steady-state voltage values expected from the FPGA portion of the Arria 10 SoC devices.

DC Characteristics

This section lists the following specifications:

- Supply Current and Power Consumption
- I/O Pin Leakage Current
- Bus Hold Specifications
- OCT Specifications
- Pin Capacitance

The OCT variation after power-up calibration specifications will be available in a future release of the *Arria 10 Device Datasheet*.

Supply Current and Power Consumption

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

Use the Excel-based Early Power Estimator (EPE) before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 7 lists the Arria 10 I/O pin leakage current specifications.

Table 7. I/O Pin Leakage Current for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Note to Table 7:

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

Bus Hold Specifications

Table 8 lists the Arria 10 device bus hold specifications. The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 8. Bus Hold Parameters for Arria 10 Devices—*Preliminary*

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 9 lists the Arria 10 OCT termination calibration accuracy specifications. The OCT calibration accuracy is valid at the time of calibration only.

Table 9. OCT Calibration Accuracy Specifications for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, and 60-Ω R_S	Internal series termination with calibration (34-Ω, 40-Ω, 48-Ω, and 60-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, and 40-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 10 lists the Arria 10 OCT without calibration resistance tolerance to PVT changes.

Table 10. OCT Without Calibration Resistance Tolerance Specifications for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5	±25	±35	±40	%
		V_{CCIO} = 1.2	±25	±35	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5	±25	±35	±40	%
		V_{CCIO} = 1.2	±25	±35	±40	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	±25	±35	±40	%

Equation 1 shows the equation to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration (1), (2), (3), (4), (5), (6)—*Preliminary*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value calculated from Equation 1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Pin Capacitance

Table 11 lists the Arria 10 pin capacitance.

Table 11. Pin Capacitance for Arria 10 Devices—*Preliminary*

Symbol	Description	Value	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	2.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	2.5	pF

Internal Weak Pull-Up Resistor

Table 12 lists the weak pull-up resistor values for Arria 10 devices.

All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. For more information about the pins that support internal weak pull-up and internal weak pull-down features, refer to the *Arria 10 Device Family Pin Connection Guidelines*.

Table 12. Internal Weak Pull-Up Resistor Values for Arria 10 Devices—*Preliminary*

Symbol	Description	Condition (V) (1)	Value (2)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 12:

(1) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(2) Valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 13 through Table 18 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

For an explanation of terms used in Table 13 through Table 18, refer to "Glossary" on page 1–46.

Table 13. Single-Ended I/O Standards for Arria 10 Devices—*Preliminary* (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Table 13. Single-Ended I/O Standards for Arria 10 Devices—*Preliminary* (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Note to Table 13:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.0-V LVTTL** specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria 10 Devices—*Preliminary*

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.31	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V_{CCIO}	0.5 x V_{CCIO}	0.53 x V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 x V_{CCIO}	0.7 x V_{CCIO}	0.71 x V_{CCIO}	—	V_{CCIO}	—

Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria 10 Devices—*Preliminary* (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{oI} (1) (mA)	I_{oh} (1) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—

Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria 10 Devices—*Preliminary* (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (1) (mA)	I_{oh} (1) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 x V_{CCIO}	0.9 x V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) x V_{CCIO}	(0.7 + 0.15) x V_{CCIO}	—	—

Note to Table 15:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **SSTL15CI** specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 16. Differential SSTL I/O Standards for Arria 10 Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15
SSTL-135	1.283	1.35	1.45	0.18	(1)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15
SSTL-125	1.19	1.25	1.31	0.18	(1)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15
POD12	1.16	1.2	1.24	0.16	—	0.3	—	V_{REF} – 0.08	—	V_{REF} + 0.08

Note to Table 16:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 17. Differential HSTL and HSUL I/O Standards for Arria 10 Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	0.3	V_{CCIO} + 0.48	—	0.5 x V_{CCIO}	—	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} +0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}

Table 18. Differential I/O Standard Specifications for Arria 10 Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (1)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (2)			V_{OCM} (V) (2)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the **CML** I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23.														
LVDS (3)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} >700 Mbps	1.6						
RSDS (HIO) (4)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (5)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	600	1	1.2	1.4
LVPECL (6)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} >700 Mbps	1.6						

Notes to Table 18:

(1) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(2) R_L range: $90 \leq R_L \leq 110\ \Omega$

(3) For optimized **LVDS** receiver performance, the receiver voltage input range must be within 1.0V to 1.6V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.

(4) For optimized **RSDS** receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.

(5) For optimized **Mini-LVDS** receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.

(6) For optimized **LVPECL** receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Switching Characteristics

This section provides performance characteristics of Arria 10 core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Table 19, Table 20, Table 21, and Table 22 describe transceiver performance specifications.

Table 19. Transceiver Performance for Arria 10 GX/SX Devices—*Preliminary*

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Transceiver Speed Grade 5	Unit
Transmitter and Receiver Data Rate							
Chip-to-chip (1)	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 1.0$ V	17.4	15	14.2	12.5	8	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 0.9$ V	11.3	11.3	11.3	11.3	8	Gbps
	Minimum Data Rate	611/125 (2)					Mbps
Backplane (1)	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 1.0$ V	16	14.2	12.5	10.3125	6.5536	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 0.9$ V	10.3125	10.3125	10.3125	10.3125	6.5536	Gbps
	Minimum Data Rate	611/125 (2)					Mbps
ATX PLL							
Supported Output Frequency	Maximum frequency	8.7	7.5	7.1	6.25	4	GHz
	Minimum frequency	500					MHz
Fractional PLL							
Supported Output Frequency	Maximum frequency	6.25	6.25	6.25	6.25	4	GHz
	Minimum frequency	305.5					MHz
CMU PLL							
Supported Output Frequency	Maximum frequency	8.7	7.5	7.1	6.25	4	GHz
	Minimum frequency	305.5					MHz

Notes to Table 19:

(1) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(2) Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

Table 20. High-Speed Serial Interface-Fabric Interface Performance for Arria 10 GX/SX Devices—Preliminary

Symbol/Description	Conditions	Core Speed Grade with Power Options				Units
		-1M (1)	-1 (2)	-2	-3	
20-bit interface - FIFO	V_{CC}= 0.9	516	516	400	400	MHz
20-bit interface - Registered	V_{CC}=0.9	491	491	400	400	MHz
32-bit interface - FIFO	V_{CC}=0.9	441	441	404	335	MHz
32-bit interface - Registered	V_{CC}=0.9	441	441	404	335	MHz
64-bit interface - FIFO	V_{CC}=0.9	272	272	234	222	MHz
64-bit interface - Registered	V_{CC}=0.9	272	272	234	222	MHz
PCIe Gen3 HIP-Fabric interface	V_{CC}=0.9	300	300	250	250	MHz
20-bit interface - FIFO	V_{CC}=0.83	400	N/A	N/A	N/A	MHz
20-bit interface - Registered	V_{CC}=0.83	400	N/A	N/A	N/A	MHz
HSSI-Fabric 32-bit interface - FIFO	V_{CC}=0.83	335	N/A	N/A	N/A	MHz
32-bit interface - Registered	V_{CC}=0.83	335	N/A	N/A	N/A	MHz
64-bit interface - FIFO	V_{CC}=0.83	222	N/A	N/A	N/A	MHz
64-bit interface - Registered	V_{CC}=0.83	222	N/A	N/A	N/A	MHz
PCIe Gen3 HIP-Fabric interface	V_{CC}=0.83	250	N/A	N/A	N/A	MHz

Notes to Table 20:

(1) -1M = -1 core speed grade devices with the V_{CC} PowerManager feature.

(2) Does not apply to -1M devices.

Table 21. Transceiver Performance for Arria 10 GT Devices—*Preliminary* (Part 1 of 2)

Symbol/Description	Condition		Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Transmitter and Receiver Data Rate						
Chip-to-chip (1)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.1 V	GT Channel (2)	28.3	26	20	Gbps
		GX Channel	17.4	15	15	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.0 V		15	14.2	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.9 V		11.3	11.3	11.3	Gbps
	Minimum Data Rate		611/125 (3)			Mbps

Table 21. Transceiver Performance for Arria 10 GT Devices—*Preliminary* (Part 2 of 2)

Symbol/Description	Condition		Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Backplane (1)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.1 V		17.4	14.2	14.2	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.0 V		14.2	12.5	10.3125	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.9 V		10.3125	10.3125	10.3125	Gbps
	Minimum Data Rate		611/125 (3)			Mbps
ATX PLL						
Supported Output Frequency	Maximum frequency		14.05	13	10	GHz
	Minimum frequency		500			MHz
Fractional PLL						
Supported Output Frequency	Maximum frequency		6.25	6.25	6.25	GHz
	Minimum frequency		305.5			MHz
CMU PLL						
Supported Output Frequency	Maximum frequency		8.7	7.5	7.5	GHz
	Minimum frequency		305.5			MHz

Notes to Table 21:

(1) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(2) GT channels are only available when V_{CCT_GXB} = 1.1V and V_{CCR_GXB} = 1.1V.

(3) Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

Table 22. High-Speed Serial Interface-Fabric Interface Performance for Arria 10 GT Devices—Preliminary

Symbol/Description	Conditions	Core Speed Grade with Power Options			Units
		-1	-2	-3	
20-bit interface - FIFO	V_{CC}= 0.9	516	400	400	MHz
20-bit interface - Registered	V_{CC}=0.9	491	400	400	MHz
32-bit interface - FIFO	V_{CC}=0.9	441	404	335	MHz
32-bit interface - Registered	V_{CC}=0.9	441	404	335	MHz
64-bit interface - FIFO	V_{CC}=0.9	439	407	313	MHz
64-bit interface - Registered	V_{CC}=0.9	439	407	313	MHz
PCIe Gen3 HIP-Fabric interface	V_{CC}=0.9	300	250	250	MHz

Table 23 lists the Arria 10 transceiver specifications.

Table 23. Transceiver Specifications for Arria 10 GX, SX, and GT Devices—*Preliminary* (Part 1 of 3)

Symbol/ Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Reference Clock					
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Rise time	20% to 80%	—	—	250	ps
Fall time	80% to 20%	—	—	250	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV

Table 23. Transceiver Specifications for Arria 10 GX, SX, and GT Devices—*Preliminary* (Part 2 of 3)

Symbol/ Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) (8)	100 Hz	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	10 kHz to 1.5 MHz (PCIe)	—	—	3	ps (rms)
R_{REF}	—	—	2.0K ±1%	—	Ω
Transceiver Clocks					
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	MHz
reconfig_clk	Reconfiguration interface	—	100	—	MHz
Receiver					
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin (1)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (9)	—	—	—	1.6	V
Minimum differential eye opening at receiver serial input pins (7)	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
	120-Ω setting	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	Ω
t_{LTR} (2)	—	—	—	10	µs
t_{LTD} (3)	—	4	—	—	µs
t_{LTD_manual} (4)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (5)	—	15	—	—	µs
Run Length	—	—	—	200	UI

Table 23. Transceiver Specifications for Arria 10 GX, SX, and GT Devices—*Preliminary* (Part 3 of 3)

Symbol/ Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
CDR PPM tolerance	PCIe-only	—	—	300	± PPM
	All other protocols	—	—	1000	± PPM
Transmitter					
Supported I/O Standards	—	High Speed Differential I/O			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	Ω
Rise time (6)	20% to 80%	30	—	160	ps
Fall time (6)	80% to 20%	30	—	160	ps
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

Notes to Table 23:

(1) The device cannot tolerate prolonged operation at this absolute maximum.

(2) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(3) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(4) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(5) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(6) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(7) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(8) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(9) DC coupling specifications are pending silicon characterization.

Figure 1. CTLE Response in High Gain Mode for Arria 10 Devices with Data Rates ≥ 8 Gbps

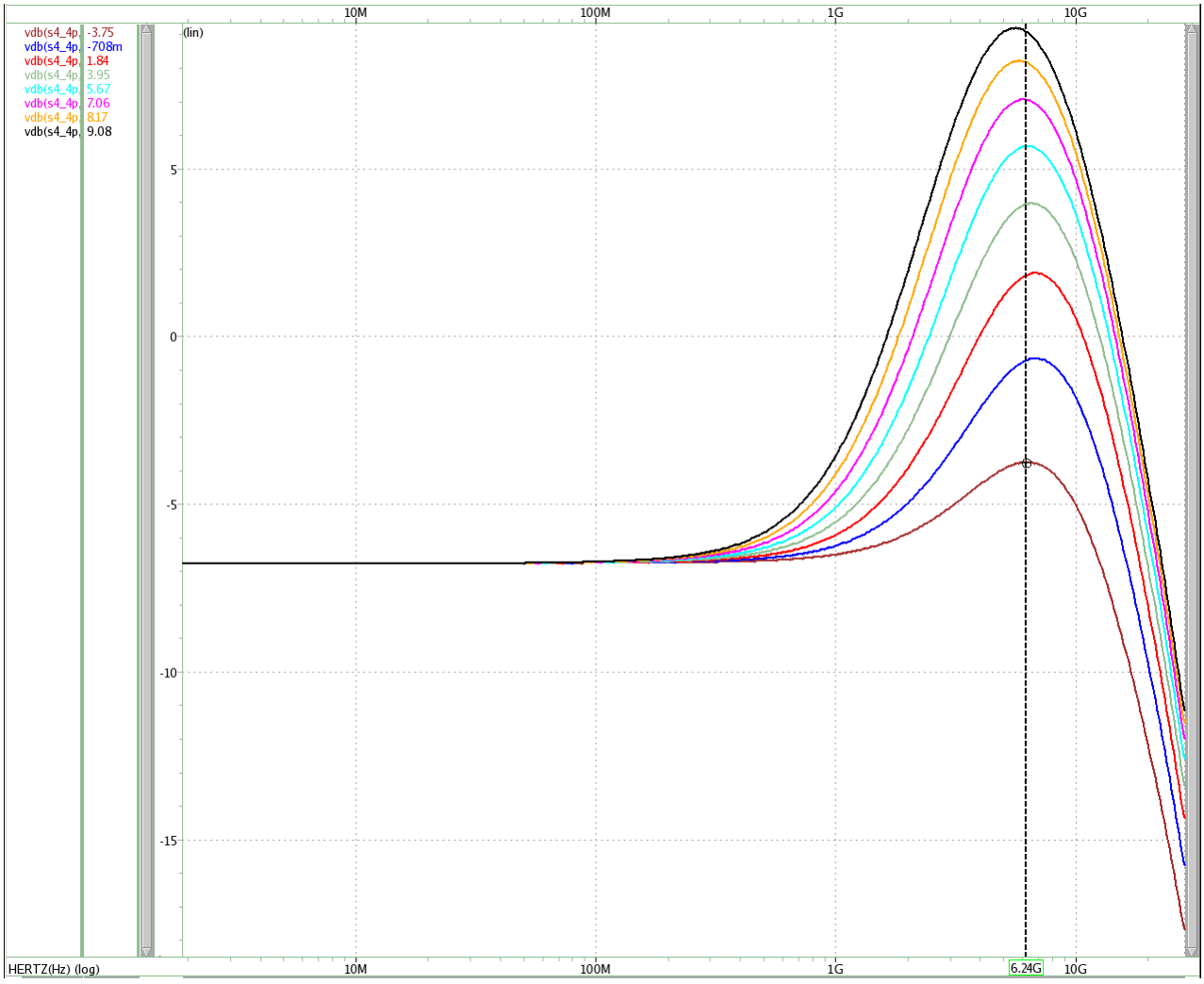
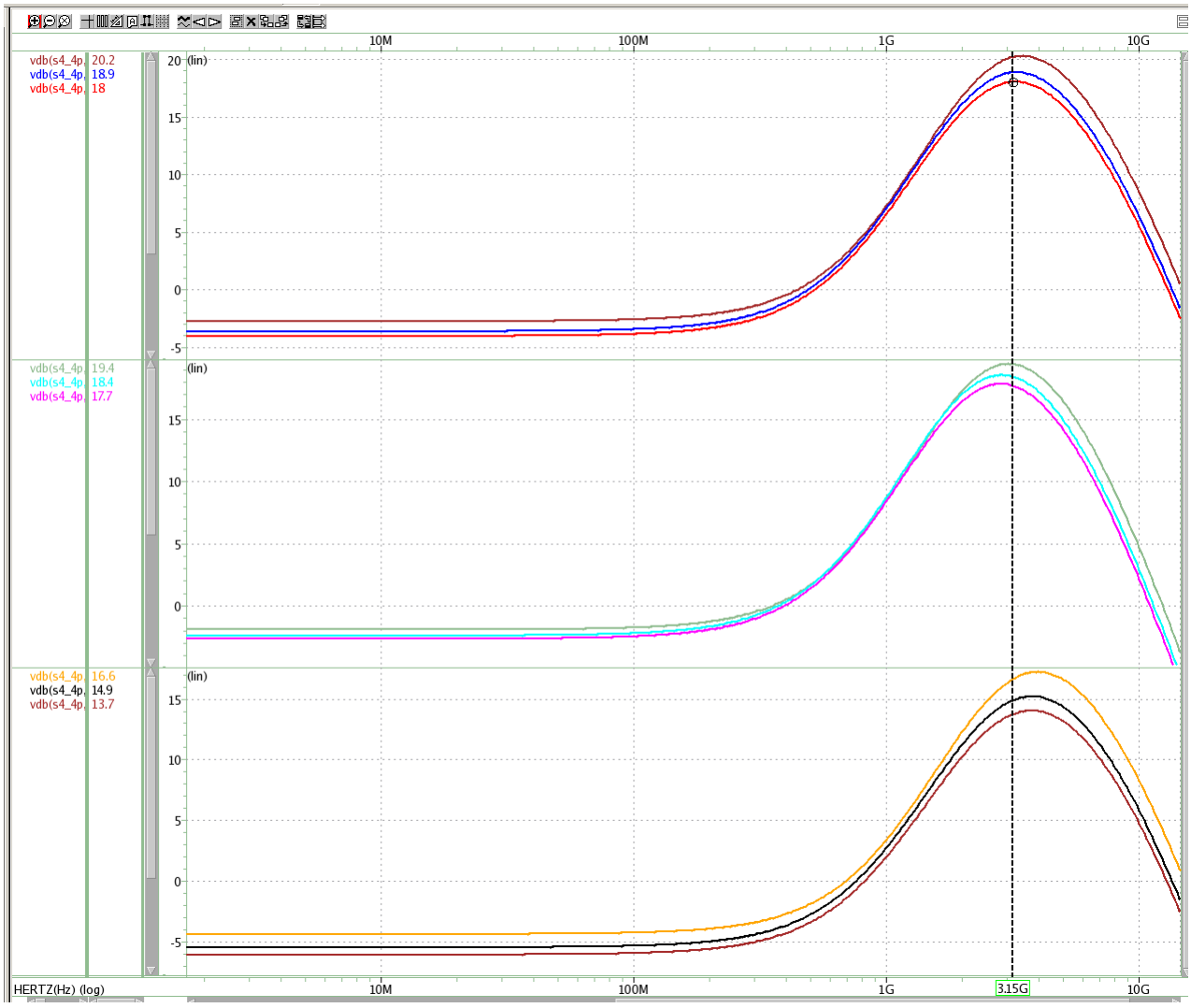


Figure 2. CTLE Response in High Gain Mode for Arria 10 Devices with Data Rates < 8 Gbps



Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, temperature sensing diode, and voltage sensor specifications.

Clock Tree Specifications

Table 24 lists the clock tree specifications for Arria 10 devices.

Table 24. Clock Tree Performance for Arria 10 Devices—*Preliminary*

Parameter	Performance			Unit
	–E1L,–E1M (1), –E1S, –I1L, –I1M (1)	–E2L, –I2L	–E1M (2), –I1M (2), –E3S, –I3S	
Global clock, regional clock, and small periphery clock	644	644	644	MHz
Large periphery clock	525	525	525	MHz

Notes to Table 24:

(1) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.

(2) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

PLL Specifications

Table 25 and Table 26 list the Arria 10 PLL specifications.

Table 25. Fractional PLL Specifications for Arria 10 Devices—*Preliminary* (Part 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1 speed grade	27	—	1000 (1)	MHz
		–2 speed grade	27	—	TBD (1)	MHz
		–3 speed grade	27	—	TBD (1)	MHz
f_{FINPFD}	Fractional input clock frequency to the phase frequency detector (PFD)	—	50	—	325	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range	–1 speed grade	2.4	—	6.25	GHz
		–2 speed grade	2.4	—	6.25	GHz
		–3 speed grade	2.4	—	6.25	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	40	—	60	%
f_{OUT_C}	Output frequency for internal global or regional clock (C counter)	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz
f_{OUT_L}	Output frequency to physical medium attachment (PMA) TX or clock generation buffer (L counter)	–1 speed grade	—	—	6.25	GHz
		–2 speed grade	—	—	6.25	GHz
		–3 speed grade	—	—	6.25	GHz
$t_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk and scanclk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms

Table 25. Fractional PLL Specifications for Arria 10 Devices—*Preliminary* (Part 2 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	TBD	—	MHz
		Medium	—	TBD	—	MHz
		High	—	TBD	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (2), (3)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	TBD	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	TBD	ps (p-p)
t_{FOUTPJ_IO} (4)	Period jitter for clock output on a regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
$t_{FOUTCCJ\_IO}$ (4)	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit
k_{VALUE}	Numerator of fraction	—	—	2147483648	—	—
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	—	—	0.023	—	Hz

Notes to Table 25:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(3) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(4) External memory interface clock output jitter specifications use a different measurement method, which are available in Table 36 on page 1–33.

Table 26. I/O PLL Specifications for Arria 10 Devices—*Preliminary* (Part 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN} (1)	Input clock frequency	–1 speed grade	10	—	800	MHz
		–2 speed grade	10	—	700	MHz
		–3 speed grade	10	—	650	MHz
f_{INPFD}	Integer input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	PLL VCO operating range	–1 speed grade	600	—	1600	MHz
		–2 speed grade	600	—	1434	MHz
		–3 speed grade	600	—	1250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.1	—	8	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%

Table 26. I/O PLL Specifications for Arria 10 Devices—*Preliminary* (Part 2 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OUT_C}	Output frequency for internal global or regional clock (C counter)	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1 speed grade	—	—	TBD	MHz
		–2 speed grade	—	—	TBD	MHz
		–3 speed grade	—	—	TBD	MHz
$f_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
f_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk and scanclk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ} (2), (3)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	TBD	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	TBD	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTPJ_IO} (4)	Period jitter for clock output on the regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTCCJ_IO} (4)	Cycle-to-cycle jitter for clock output on the regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	—	—	TBD	—	Hz

Notes to Table 26:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(3) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(4) External memory interface clock output jitter specifications use a different measurement method, which are available in Table 36 on page 1–33.

DSP Block Specifications

Table 27 lists the Arria 10 DSP block performance specifications.

Table 27. DSP Block Performance Specifications for Arria 10 Devices—*Preliminary*

Mode	Performance						Unit
	–E1L, –E1M (1), –E1S	–I1L, –I1M (1)	–E2L	–I2L	–E1M (2), –E3S	–I1M (2), –I3S	
Modes using One DSP Block							
Independent 18 x 19 multiplication	520	500	420	400	360	340	MHz
Independent 27 x 27 multiplication	520	500	420	400	360	340	MHz
Two 18 x 19 multiplier adder mode	520	500	420	400	360	340	MHz
18 x 18 multiplier added summed with 36-bit input	520	500	420	400	360	340	MHz
Mode using Two DSP Blocks							
Complex 18 x 19 multiplication	520	500	420	400	360	340	MHz

Notes to Table 27:

(1) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.

(2) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Memory Block Specifications

Table 28 lists the Arria 10 memory block specifications.

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Quartus II software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 28. Memory Block Performance Specifications for Arria 10 Devices—*Preliminary* (Part 1 of 2)

Memory	Mode	Resources Used		Performance					Unit
		ALUTs	Memory	–E1L, –E1M (1), –E1S	–I1L, –I1M (1)	–E1M (2), –I1M (2)	–E2L, –I2L	–E3S, –I3S	
MLAB	Single port, all supported widths (x16/x32)	0	1	700	660	490	570	490	MHz
	Simple dual-port, all supported widths (x16/x32)	0	1	700	660	490	570	490	MHz
	Simple dual-port with read and write at the same address	0	1	460	450	330	400	330	MHz
	ROM, all supported width (x16/x32)	0	1	700	660	490	570	490	MHz

Table 28. Memory Block Performance Specifications for Arria 10 Devices—*Preliminary* (Part 2 of 2)

Memory	Mode	Resources Used		Performance					Unit
		ALUTs	Memory	–E1L, –E1M (1), –E1S	–I1L, –I1M (1)	–E1M (2), –I1M (2)	–E2L, –I2L	–E3S, –I3S	
M20K Block	Single-port, all supported widths	0	1	730	690	510	625	530	MHz
	Simple dual-port, all supported widths	0	1	730	690	510	625	530	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	550	520	410	470	410	MHz
	Simple dual-port with ECC enabled, 512 x 32	0	1	470	450	360	410	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 x 32	0	1	620	590	470	520	470	MHz
	True dual port, all supported widths	0	1	730	690	510	625	530	MHz
	ROM, all supported widths	0	1	730	690	510	680	570	MHz

Notes to Table 28:

(1) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.

(2) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Temperature Sensing Diode Specifications

Table 29 lists the internal temperature sensing diode specifications for the Arria 10 devices.

Table 29. Internal Temperature Sensing Diode Specifications for Arria 10 Devices—*Preliminary*

Temperature Range	Accuracy	Sampling Rate	Resolution
–40 to 100°C	±5°C	1 Ksps	10 bits

Internal Voltage Sensor Specifications

Table 30 lists the internal voltage sensor specifications for the Arria 10 devices.

Table 30. Internal Voltage Sensor Specifications for Arria 10 Devices—*Preliminary*

Parameter	Minimum	Typical	Maximum	Unit
Resolution	10	—	12	Bit
Sampling rate	—	—	500	Ksps
Differential non-linearity (DNL)	—	—	±1	LSB
Integral non-linearity (INL)	—	—	±3	LSB
Input capacitance	—	20	—	pF
Signal to noise and distortion ratio (SNR)	60	—	—	dB
Clock frequency	—	—	20	MHz
Unipolar Input Mode				
Input signal range for Vsigp	0	—	1.5	V
Common mode voltage on Vsign	0	—	0.25	V
Input signal range for Vsigp – Vsign	0	—	1.25	V
Bipolar Input Mode				
Input signal range for Vsigp	0	—	1.25	V
Input signal range for Vsigp – Vsign	–0.625	—	0.625	V

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 31 lists high-speed I/O timing for Arria 10 devices.

Table 31. High-Speed I/O Specifications for Arria 10 Devices (1), (2), (10)—*Preliminary* (Part 1 of 2)

Symbol	Condition	–E1L, –E1M (15), –E1S, –I1L, –I1M (15)			–E2L, –I2L			–E1M (16), –I1M (16), –E3S, –I3S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (3)	10	—	800	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (3)	10	—	625	10	—	625	10	—	TBD	MHz
f_{HSCLK_OUT} (output clock frequency)	—	—	—	800 (4)	—	—	700 (4)	—	—	625 (4)	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate) (14)	SERDES factor J = 4 to 10 (5), (6), (7)	(6)	—	1600 (8)	(6)	—	1434 (8)	(6)	—	1250 (8)	Mbps
	SERDES factor J = 3 (5), (6), (7)	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR registers	(6)	—	840 (8), (9)	(6)	—	(8), (9)	(6)	—	(8), (9)	Mbps
	SERDES factor J = 1, uses DDR registers	(6)	—	420 (8), (9)	(6)	—	(8), (9)	(6)	—	(8), (9)	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
t_{DUTY} (13)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL} (7), (11)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
TCCS (13), (14)	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps

Table 31. High-Speed I/O Specifications for Arria 10 Devices (1), (2), (10)—*Preliminary* (Part 2 of 2)

Symbol	Condition	–E1L, –E1M (15), –E1S, –I1L, –I1M (15)			–E2L, –I2L			–E1M (16), –I1M (16), –E3S, –I3S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (5), (6), (7)	—	—	1600	—	—	1434	—	—	1250	Mbps
	SERDES factor J = 3 (5), (6), (7)	—	—	(8)	—	—	(8)	—	—	(8)	Mbps
f_{HSDR} (data rate) (without DPA) (14)	SERDES factor J = 3 to 10	(6)	—	(12)	(6)	—	(12)	(6)	—	(12)	Mbps
	SERDES factor J = 2, uses DDR registers	(6)	—	(9)	(6)	—	(9)	(6)	—	(9)	Mbps
	SERDES factor J = 1, uses DDR registers	(6)	—	(9)	(6)	—	(9)	(6)	—	(9)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 31:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) For LVDS applications, you must use the PLLs in integer PLL mode.

(3) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(4) This is achieved by using the PHY clock network.

(5) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(7) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(8) Pending silicon characterization.

(9) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(11) This applies to default pre-emphasis and V_{OD} settings only.

(12) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(13) Not applicable for `DIVCLK` = 1.

(14) Requires package skew compensation with PCB trace length.

(15) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.

(16) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Figure 3 shows the DPA lock time specifications with the DPA PLL calibration option enabled.

Figure 3. DPA Lock Time Specification with DPA PLL Calibration Enabled

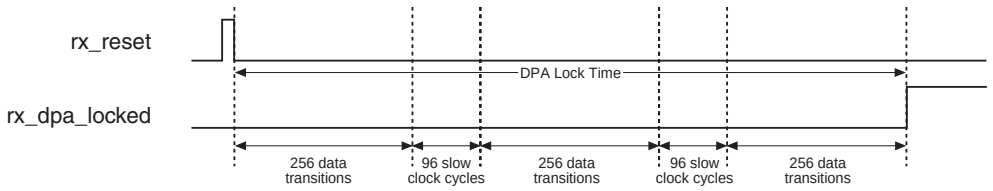


Table 32 lists the DPA lock time specifications for Arria 10 devices, which are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Table 32. DPA Lock Time Specifications for Arria 10 Devices—*Preliminary*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (1)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

Note to Table 32:

(1) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 4 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.6 Gbps.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.6 Gbps

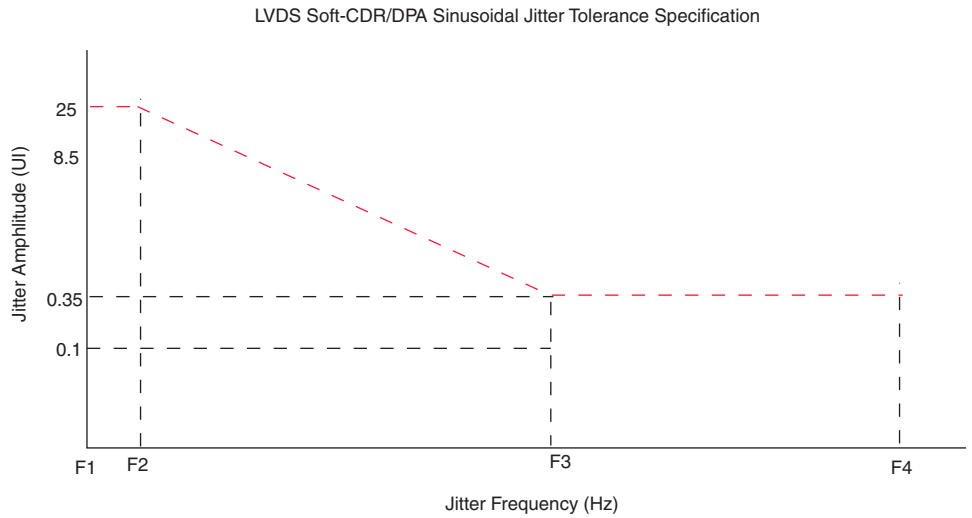


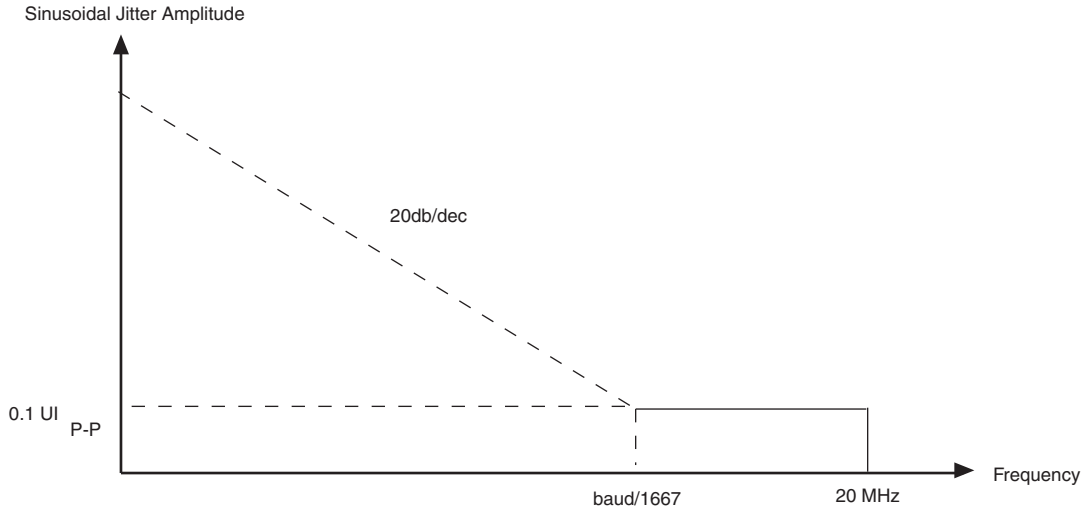
Table 33 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.6 Gbps.

Table 33. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps—*Preliminary*

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.35
F4	50,000,000	0.35

Figure 5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.6 Gbps.

Figure 5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.6 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 34 lists the DLL frequency range specifications for Arria 10 devices.

Arria 10 devices support memory interface frequencies lower than 667 MHz, although the reference clock that feeds the DLL must be at least 667 MHz. To support interfaces below 667 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Table 34. DLL Frequency Range Specifications for Arria 10 Devices—*Preliminary*

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	667 – 1333	MHz

Table 35 lists the DQS phase shift error for Arria 10 devices. This error specification is the absolute maximum and minimum error.

Table 35. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria 10 Devices—*Preliminary*

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Table 36 lists the memory output clock jitter specifications for Arria 10 devices.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Altera recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Table 36. Memory Output Clock Jitter Specification for Arria 10 Devices—*Preliminary*

Parameter	Clock Network	Symbol	–E1L, –E1M (1), –E1S, –I1L, –I1M (1)		–E2L, –I2L		–E1M (2), –I1M (2), –E3S, –I3S		Unit
			Min	Max	Min	Max	Min	Max	
PHY clock	Clock period jitter	$t_{JIT(per)}$	58	58	58	58	58	58	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	58	58	58	58	58	58	ps
	Duty cycle jitter	$t_{JIT(duty)}$	58	58	58	58	58	58	ps

Notes to Table 36:

(1) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.

(2) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

OCT Calibration Block Specifications

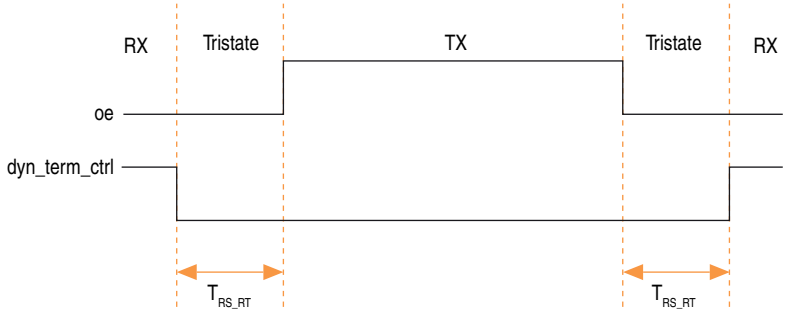
Table 37 lists the OCT calibration block specifications for Arria 10 devices.

Table 37. OCT Calibration Block Specifications for Arria 10 Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 1000		—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 6 shows the T_{RS_RT} for `oe` and `dyn_term_ctrl` signals.

Figure 6. Timing Diagram for oe and dyn_term_ctrl Signals



Configuration Specification

This section provides configuration specifications and timing for Arria 10 devices.

POR Specifications

Table 38 lists the specifications for fast and standard POR for Arria 10 devices.

Table 38. Fast and Standard POR Delay Specification for Arria 10 Devices (1)—*Preliminary*

POR Delay	Minimum	Maximum	Unit
Fast	4	12 (2)	ms
Standard	100	300	ms

Notes to Table 38:

(1) Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria 10 Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria 10 Devices* chapter.

(2) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 39 lists the JTAG timing parameters and values for Arria 10 devices.

Table 39. JTAG Timing Parameters and Values for Arria 10 Devices—*Preliminary*

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30,167 (1)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (2)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (2)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (2)	ns

Notes to Table 39:

(1) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

(2) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 11 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 11 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria 10 devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 40 lists the DCLK-to-DATA[] ratio for each combination.

Table 40. DCLK-to-DATA[] Ratio for Arria 10 Devices—*Preliminary*

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8
	On	On	8

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 7 shows the timing waveform for a FPP configuration when using a MAX® II device as an external host. This timing waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8, FPP x16, and FPP x32. For the respective DCLK-to-DATA[] ratio, refer to Table 40.

Figure 7. DCLK-to-DATA[] FPP Configuration Timing Waveform When the Ratio is 1

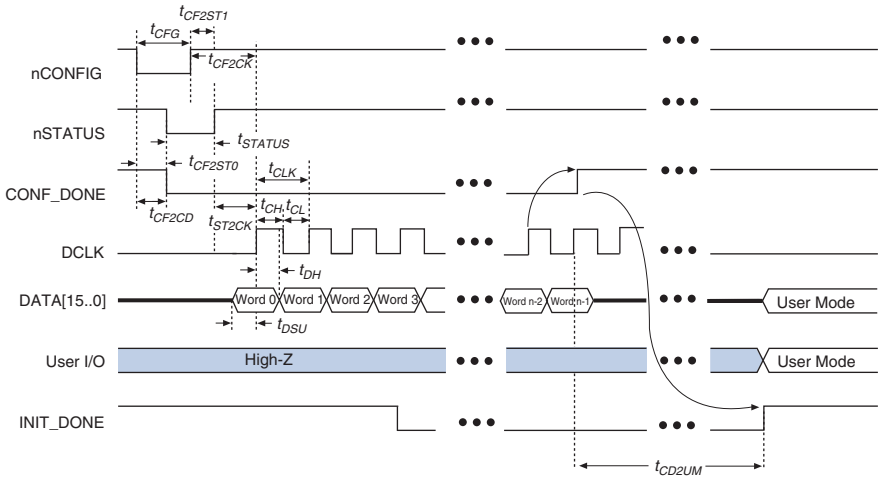


Table 41 lists the timing parameters for Arria 10 devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 41. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Arria 10 Devices (1) —*Preliminary*

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (3)	µs
t_{CF2CK} (4)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (4)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (5)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period)	—	—

Notes to Table 41:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(4) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(5) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 8 shows the timing waveform for a FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 8. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1

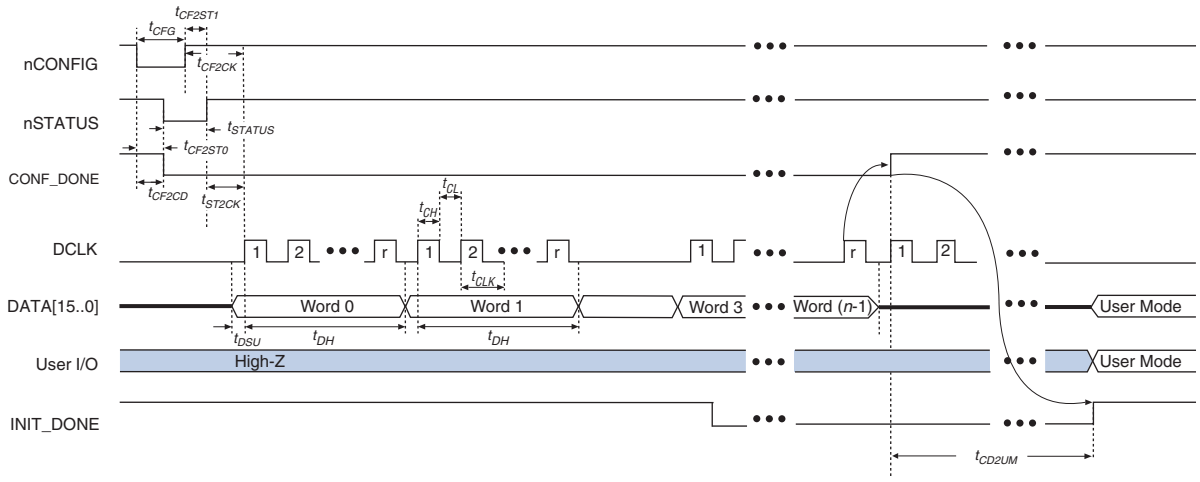


Table 42 lists the timing parameters for Arria 10 devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

Table 42. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Arria 10 Devices (1) —*Preliminary*

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (3)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (3)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	N–1/f_{DCLK} (4)	—	s
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (5)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period)	—	—

Notes to Table 42:

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(4) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

(5) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 9 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 9. AS Configuration Timing Waveform

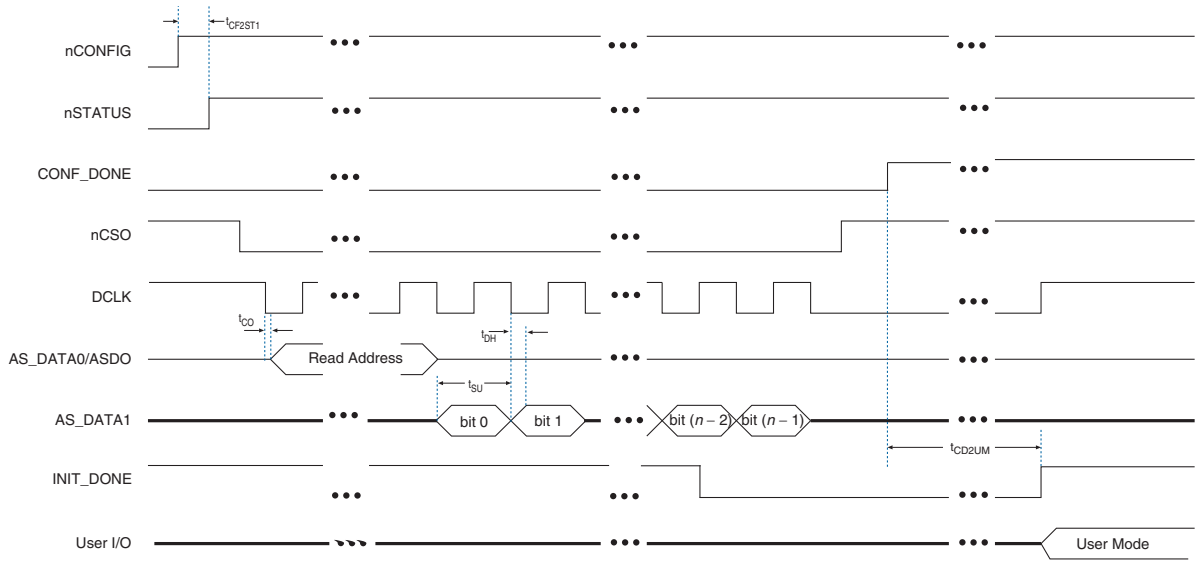


Table 43 lists the timing parameters for AS x1 and AS x4 configurations in Arria 10 devices.

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in Table 45 on page 1–42.

Table 43. AS Timing Parameters for AS x1 and AS x4 Configurations in Arria 10 Devices—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Units
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_{H}	Data hold time after falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period)	—	—

Table 44 lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Table 44. DCLK Frequency Specification in the AS Configuration Scheme—*Preliminary*

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	TBD	TBD	12.5	MHz
	TBD	TBD	25.0	MHz
	TBD	TBD	50.0	MHz
	TBD	TBD	100.0	MHz

PS Configuration Timing

Figure 10 shows the timing waveform for a PS configuration when using a MAX II device or microprocessor as an external host.

Figure 10. PS Configuration Timing Waveform

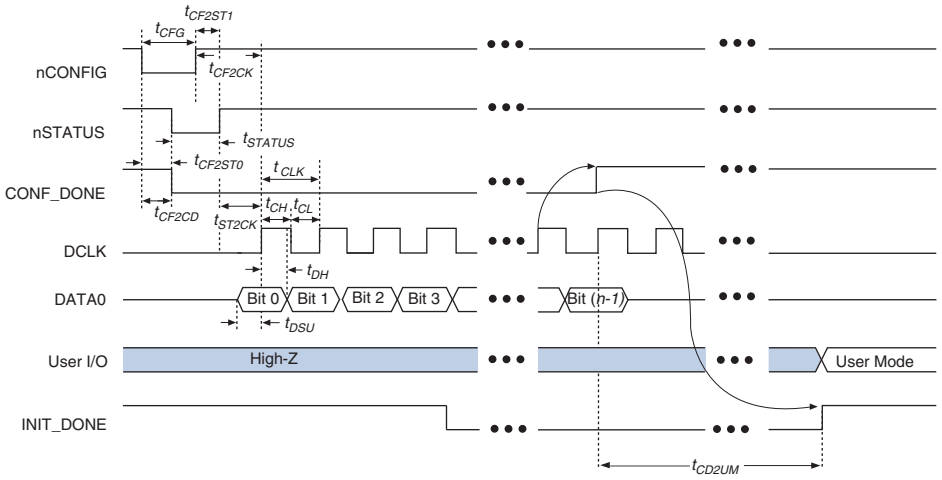


Table 45 lists the PS configuration timing parameters for Arria 10 devices.

Table 45. PS Timing Parameters for Arria 10 Devices—*Preliminary* (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (3)	nCONFIG high to first rising edge on DCLK	1,506	—	µs

Table 45. PS Timing Parameters for Arria 10 Devices—*Preliminary* (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{ST2CK} (3)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period)	—	—

Notes to Table 45:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(3) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(4) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Initialization

Table 46 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency for Arria 10 devices.

Table 46. Initialization Clock Source Option and the Maximum Frequency for Arria 10 Devices—*Preliminary*

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	TBD
CLKUSR (1)	AS, PS, and FPP	TBD	

Note to Table 46:

(1) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Use Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Arria 10 devices.

Table 47. Uncompressed .rbf Sizes for Arria 10 Devices—*Preliminary*

Variant	Product Line	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria 10 GX	GX 900	335,106,890	TBD
	GX 1150	335,106,890	TBD
Arria 10 GT	GT 900	335,106,890	TBD
	GT 1150	335,106,890	TBD

Table 48 lists the minimum configuration time estimation for Arria 10 devices. The estimated values are based on the configuration **.rbf** sizes in Table 47.

Table 48. Minimum Configuration Time Estimation for Arria 10 Devices—*Preliminary*

Variant	Product Line	Active Serial (1)			Fast Passive Parallel (2)		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria 10 GX	GX 900	4	100	837.77	32	125	83.78
	GX 1150	4	100	837.77	32	125	83.78
Arria 10 GT	GT 900	4	100	837.77	32	125	83.78
	GT 1150	4	100	837.77	32	125	83.78

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Remote System Upgrades

Table 49 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 49. Remote System Upgrade Circuitry Timing Specifications—*Preliminary*

Parameter	Minimum	Maximum	Unit
$f_{MAX\_RU\_CLK}$ (1)	—	40	MHz
$t_{RU\_nCONFIG}$ (2)	250	—	ns
$t_{RU\_nRSTIMER}$ (3)	250	—	ns

Notes to Table 49:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria 10 Devices* chapter.

(3) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria 10 Devices* chapter.

User Watchdog Internal Circuitry Timing Specification

Table 50 lists the frequency specifications for the user watchdog internal oscillator.

Table 50. User Watchdog Internal Oscillator Frequency Specifications for Arria 10 Devices—*Preliminary*

Parameter	Minimum	Typical	Maximum	Units
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The Excel-based I/O Timing spreadsheet will be available in a future release of the *Arria 10 Device Datasheet*.

Glossary

Table 51 lists the glossary for this datasheet.

Table 51. Glossary Table (Part 1 of 4)

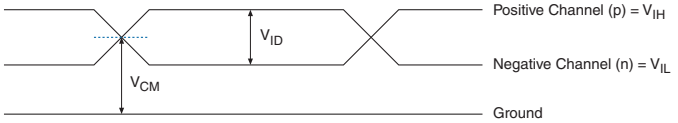
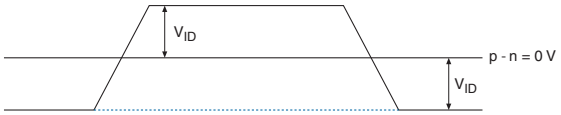
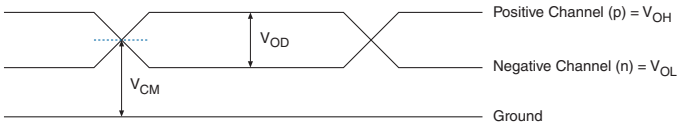
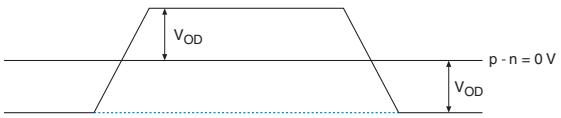
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 51. Glossary Table (Part 2 of 4)

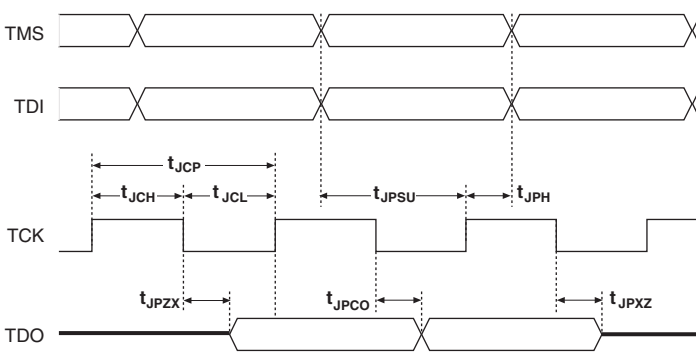
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	**Preliminary**	Some tables show the designation as “Preliminary”. Preliminary characteristics are created using simulation results, process data, and other known parameters. Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Arria 10 device).

Table 51. Glossary Table (Part 3 of 4)

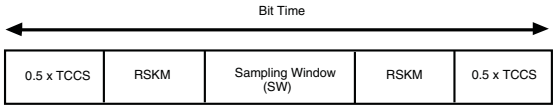
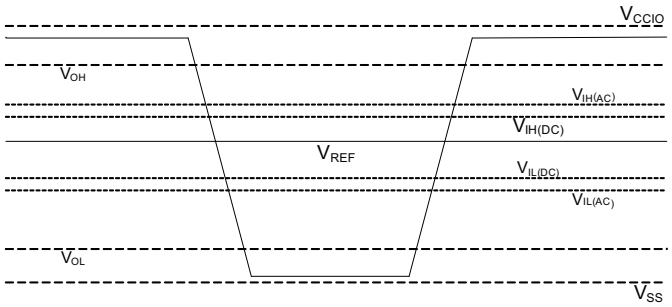
Letter	Subject	Definitions
S	**Sampling window (SW)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80–20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 51. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_{IX}	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 52 lists the revision history for this document.

Table 52. Document Revision History

Date	Version	Changes
March 2014	2014.03.14	Updated Table 3, Table 5, Table 21, Table 23, Table 24, Table 31, and Table 40.
December 2013	2013.12.06	Updated Figure 1 and Figure 2.
December 2013	2013.12.02	Initial release.